

- Q.13. In μP based systems DMA facility is required to
- increase the speed of data transfer between the μP and the I/O devices
 - increase the speed of data transfer between the μP and the memory
 - increase the speed of data transfer between the memory and the I/O devices
 - improve the reliability of the system.
- Q.14. An 8-bit microprocessor signifies that it has
- an 8-bit address bus
 - an 8-bit control bus
 - 8 interrupt lines
 - an 8-bit data bus
- Q.15. A microprocessor is capable of addressing 64K bytes of memory. Its address bus width is
- 8
 - 12
 - 16
 - 20
- Q.16. If the contents of ~~IE~~^{Ex} register is 97 H which interrupt type is disabled
- ES
 - ETI
 - E x I
 - E x O
- Q.17. In 8051, in standard ~~VART~~^{VART} SERIAL DATA Model no of bits transmitted are
- 8-bits
 - 9-bits
 - 10-bits
 - none of these
- Q.18. Internal RAM in 8051 is of capacity of
- 128 bytes
 - 128 K
 - 64 K
 - 64 Bytes
- Q.19. Which bit is used to globally enable/disable all interrupts
- GF0
 - EA
 - GF1
 - EX
- Q.20. The instruction set of μP
- is specified by the manufacturer
 - is specified by user
 - can be changed by user
 - is stored inside the μP
- Q.21. What do the contents of instruction register specify
- operand for the instruction being executed
 - Op code for the instruction being executed
 - OP code for the instruction to be executed next
 - Operand for the instruction to be executed next.
- Q.22. Serial input data of 8085 can be loaded into bit 7 of the accumulator by
- executing a RIM instruction
 - executing RST 1
 - Using TRAP
 - None of the above
- Q.23. The program ROM found in high volume microprocessor-based product most likely to be a
- mask ROM
 - PROM
 - EPROM
 - EAROM
- Q.24. Devices in a microprocessor system
- have specific addresses assigned to them
 - always respond to only single address
 - are always controlled by an address decoder circuit
 - are all of the above
- Q.25. Cache memory is logically positioned
- between CPU and main memory
 - between main memory and secondary memory
 - inside the CPU
 - inside the I/O processor.

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